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Analysis of SOI MOSFET for High Power Applications

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Abstract-

In this work, there are some changes carried out in the conventional LDMOS using silicon material known as MOS1 by utilizing trench in addition dual gate and drain architecture known as MOS2. The gate electrode is placed in SiO_2 (oxide) trenches which are located in the epi-layer at nearbyof the drain. The drain contact is positioned at the centre and topmostof the architecture. However, the sources are located at the edges of the architecture. In the proposed MOS2, twogatescreating the dual-channels. These channels acts simultaneously so give emphasis togain, drive current, resistance,and threshold voltage essential for the power ICs of the proposed structure (MOS2).A slight enlargement in breakdown occurs due to the mechanism of RESURF in MOS2. This RESURF mechanism happened with consideration of dual trenches of SiO_2. With the help of 2-D simulator the performance and characteristics are analysed, and compare the results of the trench-LDMOS (MOS2) with that of the planer MOS (MOS1). The trench architecture(MOS2) gives 13% decrease the threshold-voltage, 2.18 times higher output current, 1.34 times enhancement in breakdown voltage, and111% enhancement in gain (g_m)in comparison with the planer MOSFET.

Keywords- *Silicon; Poly Si; cut-off frequency; SiO_2.*

I. INTRODUCTION

In the today's market, the requirement is new design models and innovationsin fabrication mechanism have led to rapidprogress in semiconductor device performance. The semiconductor power device is known as laterally diffused MOS transistors (LDMOSFETs). The main advantage of LDMOSFET structures issimple integration withdifferent architectures i. e. RF MOSFET, analog/digitalMOSFET, and power transistors to obtain a singleintegrated circuits (ICs) for various applications such as remote sensing driver,microwave ICs,supplies in the computer processors, digital switching circuits, satellite-sensing device, and optic-electronic devices.The n-channel LDMOS becomes very popular due to abundance availability in the nature and high performance in high power circuits. The advantage of high e^- mobility, low energy band gap n-channel SiLDMOS make these transistors a suitable candidate for VLSI and high speed applications. Intoday's competitive market researchers observed thatSi-MOSFETs acts as a key ingredient for future electronics industry. From the past few decades and till today's market Si is used as a popular material in semiconductor industry for manufacturing various e-products. Themain advantage is good oxide-Si interface, for the development of LDMOSFETs with silicon channel. Due to the good oxide interface Si acts as an emerging semiconductor material. For high voltage applications, the semiconductor device should exhibit high drain current, maximum (i. e.

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Vol-22-Issue-34-December -2019

peak) gain, large ratio of thecurrent (On/Off), low-leakage, and high gain. Although, high gate-dielectrics of SiO_2exhibit maximum current value at small drain potential with satisfactory short channel effects. Therefore, it is very challenging task for scientists and academicians to realise improvement simultaneously in all parameters.In this research, we propose Siarchitecture (MOS2) by introducing trench concept that can bring significant progresses in the performing parameters over the MOS1. Simulations are accomplished by using ATLAS, the performance of the Si LDMOS (MOS2) has been reviewed andalso a comparison is accomplished with the MOS2.

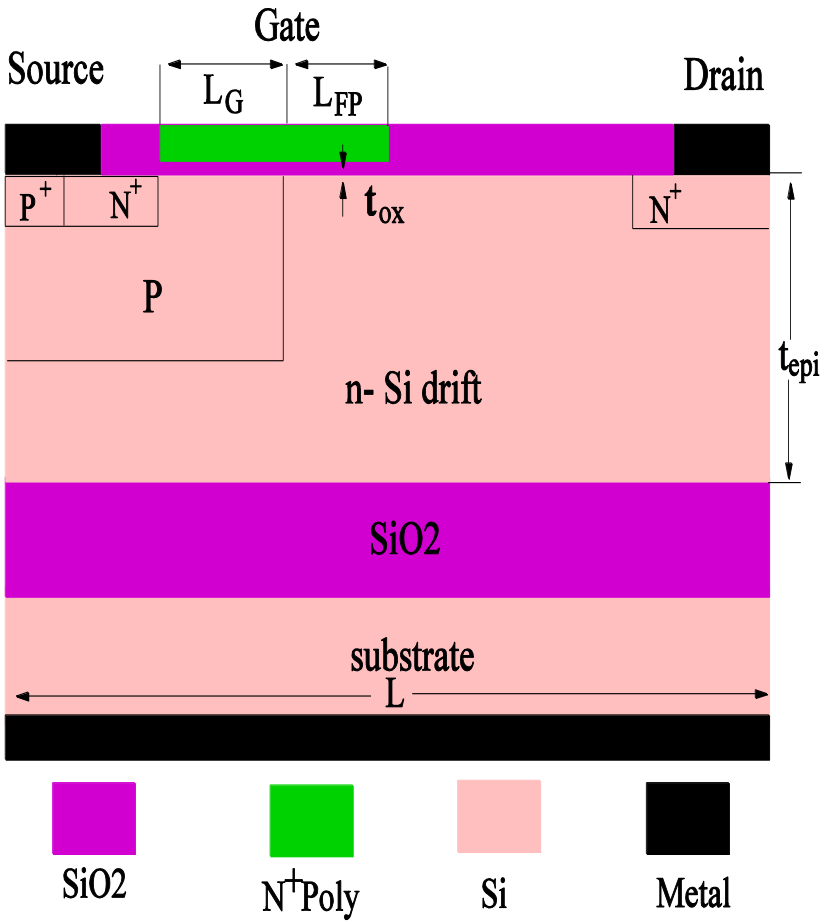

Fig. 1. Cross-sectional view of the MOS1

ISSN:0971-1260
Vol-22-Issue-34-December -2019

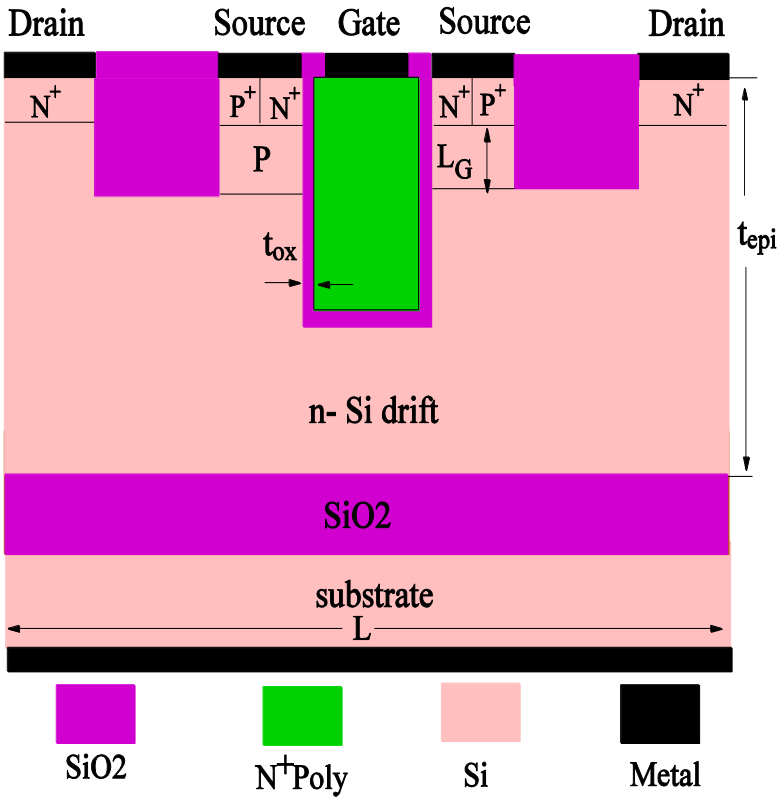

Fig. 2. Cross-sectional view of MOS2

II. MOSFETARCHITECTURE ANALYSIS

The schematic view of the planer MOS (MOS1) and proposed MOS (MOS2) devices are shown in Fig. 1 and 2, respectively. Devices are implemented on Si material. In both the MOSFETs, SiO_2 acts as insulating material and lightly doped Si is considering as substrate material. The gate electrode is made by utilizing poly-Si material.The gate is extended towardsthe x-axes so it acts as field-plate. The advantage is minimising the field lines so maximise the breakdown(BV). In the MOS1 device,at theend of the overextended gate breakdown happens in the drift layer. In the simpleLDMOS (MOS1), only one channel is formed and the small amount of currentis flows through the drift layer so increase the resistance value. These problems are overcomeby the MOS2architecture isshown in Fig. 2. In the proposed architecture MOS2, gate contact issituatedin anoxide (SiO_2) trench which is placed at the centre of structure. Furthermore, twovertical trenchesfilled with SiO_2 are situated oneither sides of gate contact. At the adjacent of oxide trenches the drain electrodes are placed. In the MOS2 parallel conduction of current occurs in the p-body of device. The flow of current is vertical in direction from drain to sourcevia the bulk of drift layer simultaneously.Hence, the drain-current and peak value of gain of the MOS2enhance due to superiorgate-control mechanism over the drive current. In the MOS2 channels act in parallel mechanism so the threshold potential and the value of resistancedrops. This conduction is helpful to raise the drain current value.The reduced-surface field (RESURF)influence happens in the MOS2 with the consideration of trenches so minimising the fieldwhich gives the large breakdown (BV). The MOS2 structure contains two channel and two oxide trenches so itoffersmany benefit over all the parameters than theMOS1. Table-I consists of MOS1 and MOS2 parametersused in the simulation.

ISSN:0971-1260
Vol-22-Issue-34-December -2019

TABLE I

PARAMETERS OF THE MOS1 AND MOS2

MOS Parameters	MOS1	MOS2
MOS length	5 micro-meter	5 micro-meter
Gate length	0.5 micro-meter	0.5 micro-meter
Field length	1 micro-meter	-
Oxide thickness	30 Nano-meter	30 Nano-meter
P-body doped	7×10^{16} cm^{-3}	7×10^{16} cm^{-3}
Drift-region doped	2.0×10^{16} cm^{-3}	2.0×10^{16} cm^{-3}
Epi-layer thickness	0.7 micro-meter	2.1 micro-meter

III. ANALYSIS OF THE OUTCOMES

The MOS1 and MOS2 structures were implemented with the help of ATLAS and simulations are carried out by considering suitable models such as CONMOB, FLDMOB, and SRH [13]. The characteristics of the MOS1 and MOS2 structures are compared below.

A. I_D-V_D Characteristics

The I_D-V_D characteristics of the MOS1 and MOS2 at various inputpotentials are depicted in Fig. 3. From the I-V characteristics,the current ability of the MOS2 is considerably higher than the MOS1 for all gate potentials. At input bias of 1.5 V, the value of the saturated output current of the MOS2 and MOS1 are 0.07 and 0.032 mA/μm, respectively. The result indicates the output drive current value of the MOS2 is 2.18 times higher in contrast to MOS1. To achieve a desired current, the MOS2 will require less width as compared to MOS1 and this is one advantage of MOS2 in term of fabrication area. Therefore, overall the cost advantage of the MOS2 over the MOS1.

ISSN:0971-1260
Vol-22-Issue-34-December -2019

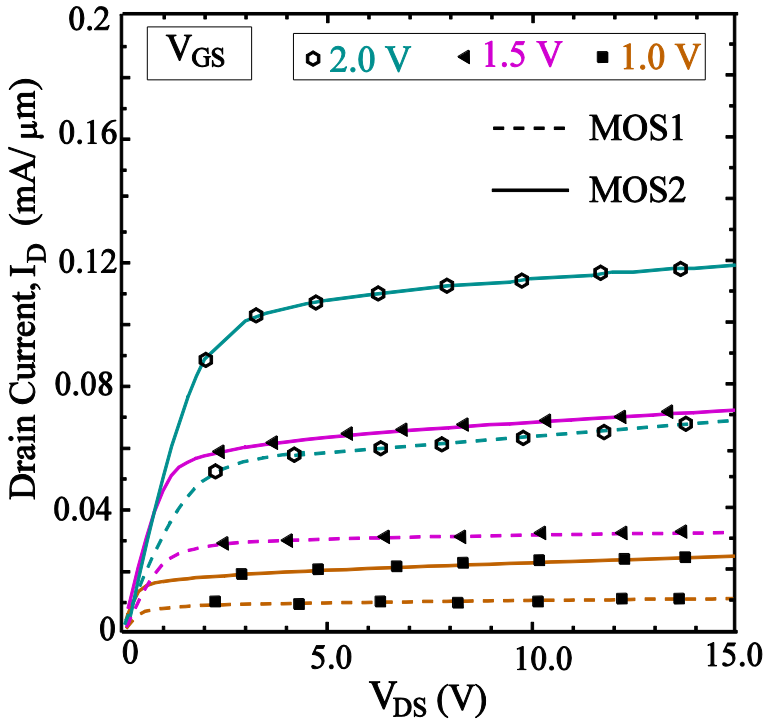

Fig. 3. I-V characteristics of the MOS1 and MOS2.

B. ThresholdCurves Analysis

The transfer curves of MOS2 and MOS1 are depicted in Fig. 4. For the extraction of threshold voltage, drawn a tangent line, at the point of the extreme slope of the curve exist on the input potential axis (V_{GS}). The value of threshold potential in the MOS2 and MOS1 are detected 0.85 and 0.98 volt, respectively. It signifies that the MOS2 consist 13% decrease in threshold potential over the MOS1.

ISSN:0971-1260
Vol-22-Issue-34-December -2019

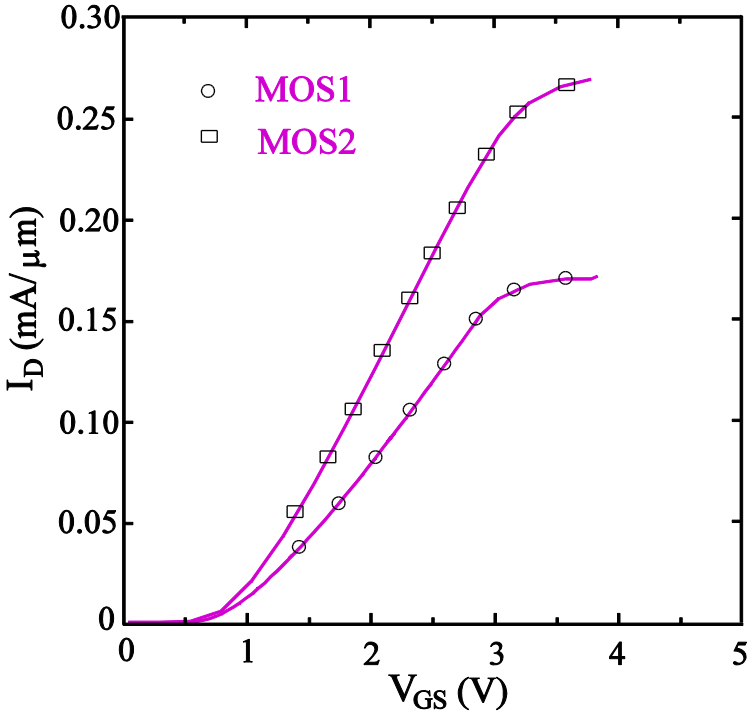

Fig. 4. Transfer curves of the MOS1 and MOS2

C. Transconductance Analysis

Fig. 5 depicted the variation of g_m (gain) with input potential of the MOS2 and MOS1. It is

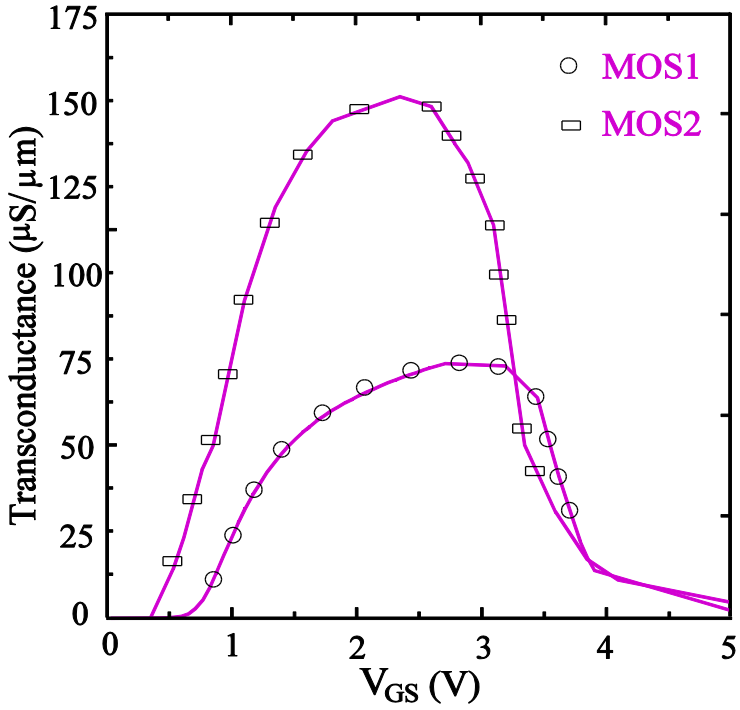

Fig. 5. Transconductance curves of the MOS1 and MOS2

observed that the MOS2 demonstrates higher g_m as compared to the MOS1. Therefore, MOS2 represents good control of gate over the drive current. The g_m value of the T-MOS2is

ISSN:0971-1260
Vol-22-Issue-34-December -2019

151.5µS/µm and MOS1 is 72µS/µm. MOS2 gives 111% enhancement in gain. This is due to the fast current conduction phenomenon. Higher the value of $g_m$makes the MOS2 a better candidate for future VLSI technology and microwave applications.

D. Breakdown (BV)Analysis

The BV characteristics of MOS1and MOS2 are depicted in Fig. 7. The BV characteristics are observed at V_{DS} = 0 V. The BV for MOS1 is 63 V and BV for MOS2 is 85 volt. MOS2 consists 1.34 times higher the BV as compared MOS1.In MOS2 this effect happens due tofall offield value in the drift region. Hence, MOS2 is suitable for high power applications.

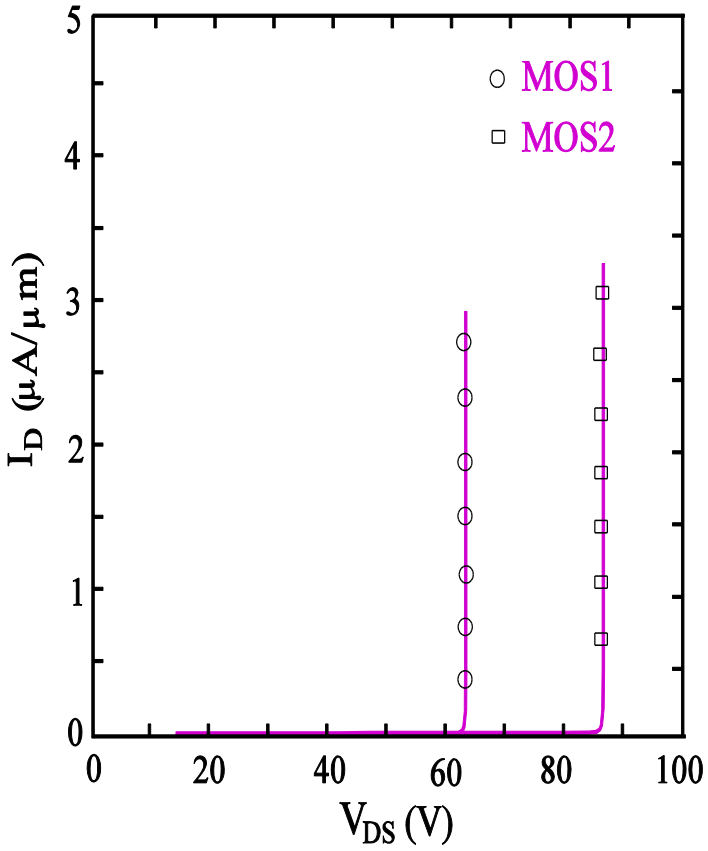

Fig. 7. Breakdown of the MOS1 and MOS2

IV. CONCLUSION

A new n-channel Si LDMOS (MOS2) with trench technology is demonstrated. The MOS2 consists of good current conduction in order to obtain the considerable enhancements in transconductance (i. e. g_m), output drive current (i. e. I_D), and cut-off frequency (i. e. f_T) for satellite and radio-frequency applications. With the help of 2D simulator analysis, the MOS2 architecture demonstrated to obtain 2.18 times higher drive current, 111% enhancement in gain, 1.34 times higher BV, and 13% reduction in threshold voltage in comparison to the MOS1. All the results indicate that substantial enhancements in semiconductor device

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Vol-22-Issue-34-December -2019

(MOS2) performance parameters can be achieved at the cost of some extra processing steps. The MOS2 architecture is a suitable candidate for future PICs and high voltage applications.

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